

Sensored Single-Phase BLDC Motor Driver Using PIC16F1613

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INTRODUCTION

This application note describes a driver solution for single winding single-phase BLDC, based on the PIC16F1613 microcontroller. The driver exploits two feedback loops: the inner loop, which is responsible for the commutation control, and the outer loop which is responsible for the speed control. The speed of the motor is referenced to an external analog voltage. Fault detection can be sensed during overcurrent and overtemperature conditions.

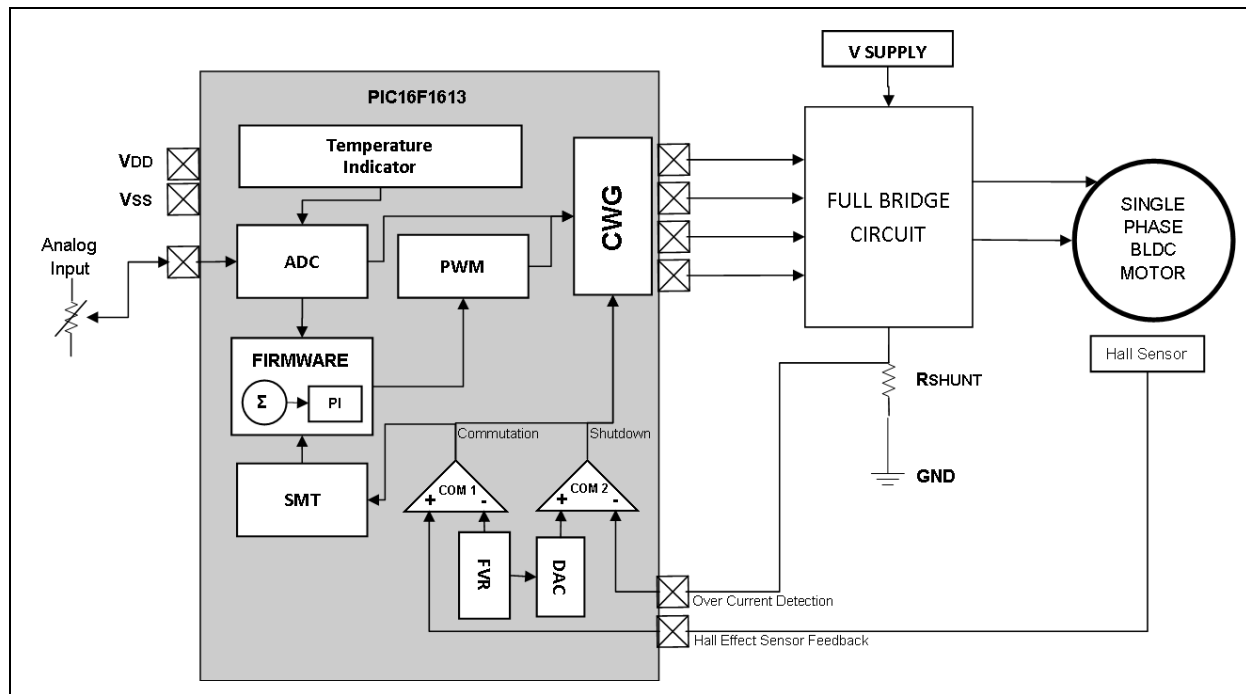
BLOCK DIAGRAM

Figure 1 shows the block diagram of a single-phase BLDC driver based on the PIC16F1613 microcontroller. The peripherals used in the application are:

- Complementary Waveform Generator (CWG)
- Signal Measurement Timer (SMT)
- Analog-to-Digital Converter (ADC)
- Digital-to-Analog Converter (DAC)
- Capture Compare PWM (CCP)
- Fixed Voltage Reference (FVR)
- Timer 1 (TMR1)
- Comparator
- Temperature Indicator

These peripherals are internally connected by firmware, significantly reducing the number of external pins required for the implementation.

FIGURE 1: BLOCK DIAGRAM



The full-bridge circuit, which energizes the motor winding of the single-phase BLDC motor, is controlled by the CWG output. The rotor position of the motor is sensed by the Hall sensor. The current that passes through the motor winding is translated into a voltage through the sense resistor (RSHUNT) for overcurrent protection. The speed can be referenced in an external analog input. Refer to [Appendix E: “Circuit Schematic”](#) for the detailed schematic diagram.

CONTROLLING THE MOTOR

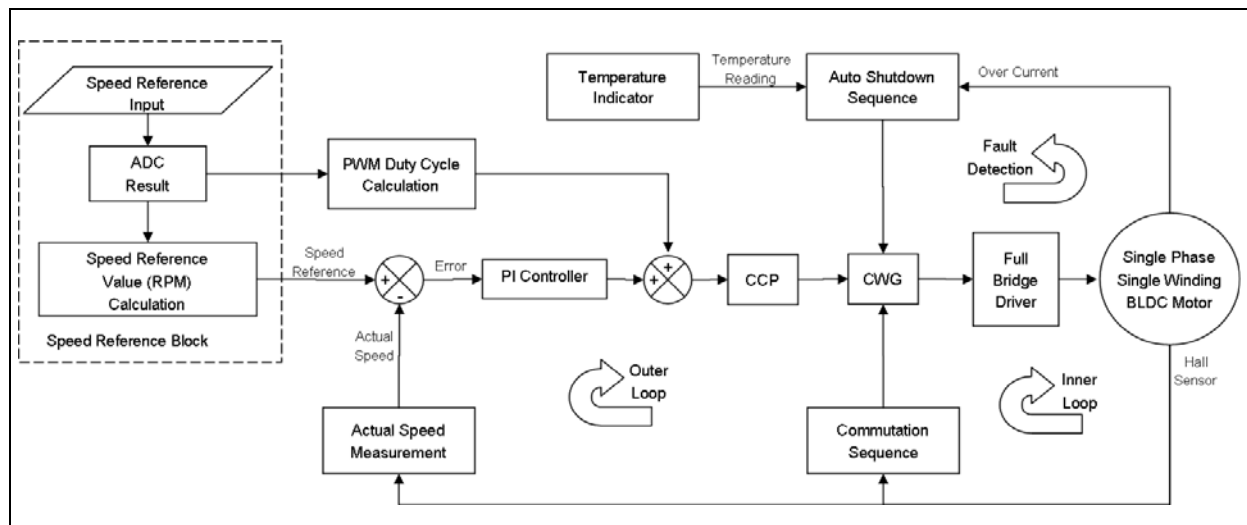
In a low-power motor application, where cost is more important than complexity and torque requirements are reduced, the single-phase Brushless Direct Current (BLDC) motor is a good alternative to a three-phase BLDC motor. This type of motor is low cost because of its simple construction, which is easier to fabricate. Also, it only requires a single-position sensor and a few numbers of driver switches in order to control and energize the motor winding. Therefore, the trade-off between motor and control electronics cost can work out favorably overall.

In maintaining the cost effectiveness of a single-phase BLDC motor application design, it is equally important to choose a low-cost, yet highly suitable motor driver controller. The PIC16F1613 8-bit microcontroller is best fit for these requirements because it is low cost, low pin count and has on-chip peripherals that are capable of controlling the driver switches, measuring the motor speed, predicting the rotor position and implementing Fault detection.

There are two types of single-phase BLDC motors: one uses a single winding and the other uses a bifilar wound construction. The former requires a full-bridge driver and the latter requires only the two low-side switches of a full-bridge driver. Both can be controlled by the PIC16F1613 microcontroller.

[Figure 2](#) shows the control diagram of the motor driver. Referring to this diagram will help explain how the driver controls the motor.

FIGURE 2: CONTROL DIAGRAM



SPEED REFERENCE

The speed reference block seen in [Figure 2](#) sets the demand speed of the motor. The higher the speed reference value, the faster the motor will spin. Calculation of the speed reference depends on the following parameters:

- Rated/Nominal Motor Voltage
- Rated/Nominal Motor Speed
- Motor Driver Supply Voltage
- Speed Reference Input

The rated motor voltage and speed can be found in the technical specifications of the motor. For this application, the rated motor voltage is 5V and the rated motor speed is 2400 RPM. The motor driver supply voltage is 9V.

The speed reference can be any analog input. The PIC16F1613 ADC module has a 10-bit resolution ADC and up to eight channels available, making it suitable for different kinds of analog input. The 10-bit ADC result will be used to derive the speed reference and the initial PWM duty cycle. [Equation 1](#) shows the speed reference calculation. The result yields a RPM (Revolution per Minute) value since speed reference is a function of the rated motor speed.

PWM Duty Cycle Calculation

The calculation of the PWM duty cycle can be obtained using [Equation 2](#). The calculated PWM duty cycle value is used to initialize the speed of the motor, based on the source of the speed reference. The initial duty cycle can be increased or reduced by the result of the PI controller. The PI controller will be discussed more in the “*Outer Feedback Loop*” section. The new duty cycle value will be loaded in CCP and the CCP's PWM output will be used as input source of CWG in order to control the modulation of lower side switches of full-bridge driver hence, the speed of the motor.

[Table 1](#) shows the range of the firmware's calculated PWM duty cycle value based on the analog input.

EQUATION 1: SPEED REFERENCE VALUE IN RPM CALCULATION

$$\text{Speed Reference (RPM)} = \frac{\text{Rated Motor Speed}}{\text{ADC Resolution}} \times (\text{ADC}_{\text{Result}})$$

EQUATION 2: PWM DUTY CYCLE CALCULATION

$$\text{PWM Duty Cycle} = \frac{\text{Rated Motor Voltage}}{\text{Supply Voltage}} \times (\text{ADC}_{\text{RESULT}})$$

TABLE 1: PWM DUTY CYCLES BASED ON ANALOG INPUTS AS SPEED REFERENCE

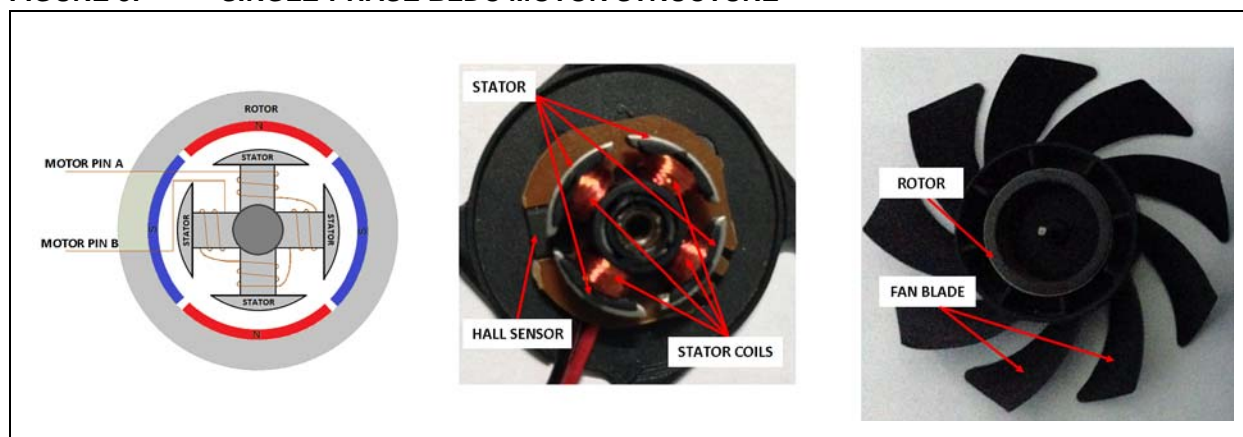
Analog Input	ADC Result	Speed Reference (RPM)	PWM Duty Cycle
5.0 V	1024	2400	569
4.5 V	922	2160	512
4.0 V	819	1920	455
3.5 V	717	1680	398
3.0 V	614	1440	341
2.5 V	512	1200	284
2.0 V	410	960	228
1.5 V	307	720	171
1.0 V	205	480	114
0.5 V	102	240	57
0 V	0	0	0

INNER LOOP

In [Figure 2](#), there are two feedback loops implemented to control the rotation of the motor. One of the loops is the Inner Feedback Loop. The inner feedback loop is responsible for the commutation control.

In a single-phase BLDC motor, a four-slot stator contains the windings and the rotor is a four-pole permanent magnet. [Figure 3](#) shows a typical structure for the single-phase BLDC Motor. The rotor is the one that produces a rotating motion. To make the rotor turn, there must be a rotating electric field. The single winding is excited to create a rotating electric field. To prevent the permanent magnet rotor from getting locked with the stator, the excitation on the stator winding must be sequenced in a specific manner, while knowing the exact position of the rotor magnets. The rotor magnet position can be determined by using Hall effect sensor.

FIGURE 3: SINGLE-PHASE BLDC MOTOR STRUCTURE



[Figure 4](#) shows the timing control based on the Hall sensor. The CWG output, which controls the excitation of the stator winding, is dependent on the state of the Hall sensor output. In order to control the CWG output by the Hall sensor, the Hall sensor output is compared with a Fixed Voltage Reference by the comparator. The comparator hysteresis is enabled to disregard the noise that might add in the sensor output. The output of the comparator toggles CWG1MODE0 bits of CWG's CWG1CON0 Register. When the bit is active, the CWG output is in Forward Full Bridge mode and when inactive, the CWG output is in Reverse Full Bridge mode. The toggling from Forward-to-Reverse mode produces a clockwise rotation, while toggling from Reverse-to-Forward mode produces a counter-clockwise rotation.

The CWG output is fed to the switches' input of the full-bridge circuit. [Figure 5](#) shows the forward and reverse full-bridge operation and the corresponding magnet polarity that the four-slot stator produces based on the CWG output. In Forward mode, Q1 is ON, Q2 and Q3 are OFF and Q4 is modulated while in Reverse mode, Q1 and Q4 are OFF, Q2 is modulated and Q3 is ON. In order to produce one electrical cycle, a forward-reverse combination must be executed. One mechanical revolution of the motor requires two electrical cycles, therefore, two forward-reverse combinations must be executed to complete a single clockwise rotation of the motor.

FIGURE 4: SENSOR AND DRIVE TIMING DIAGRAM

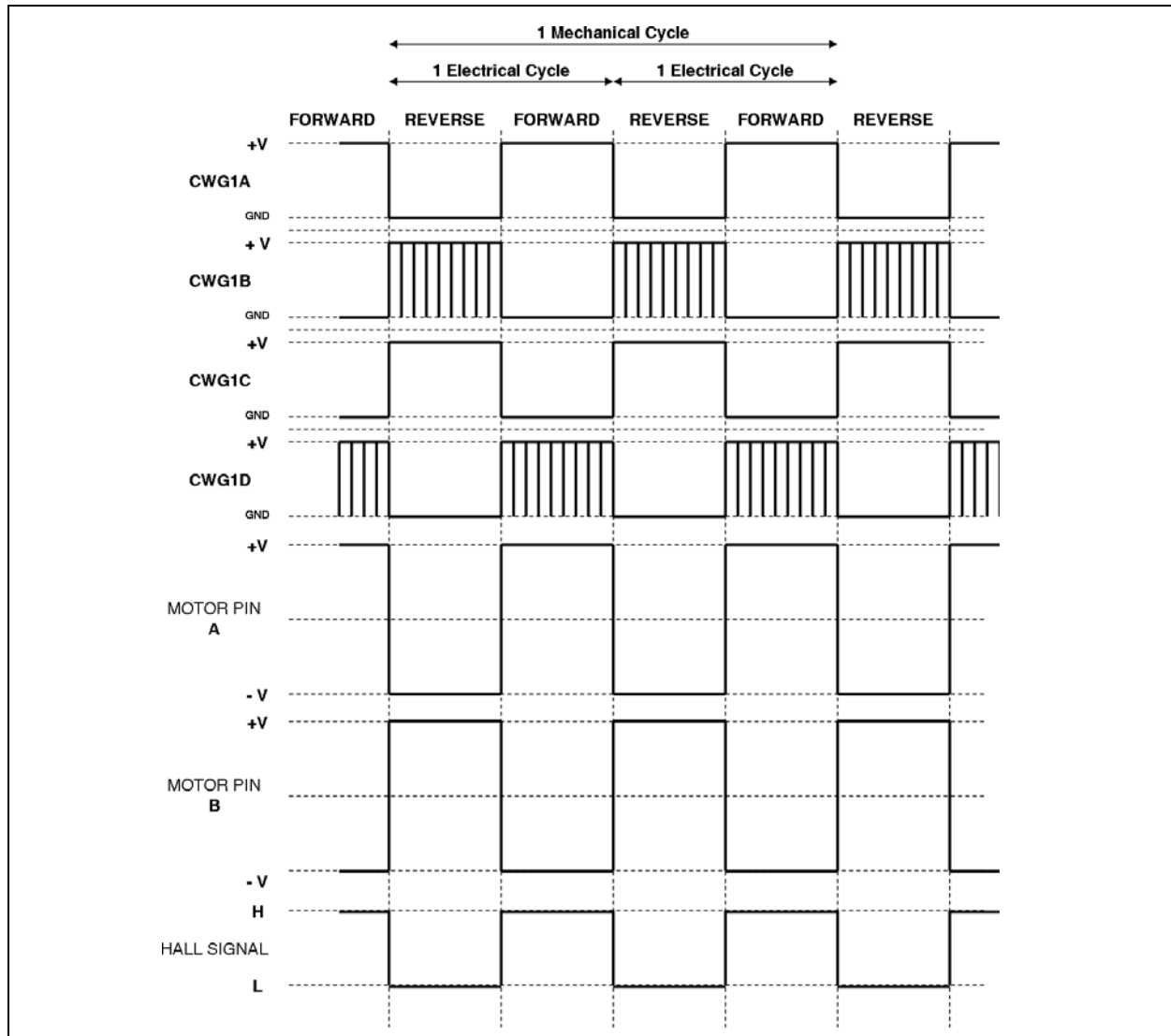
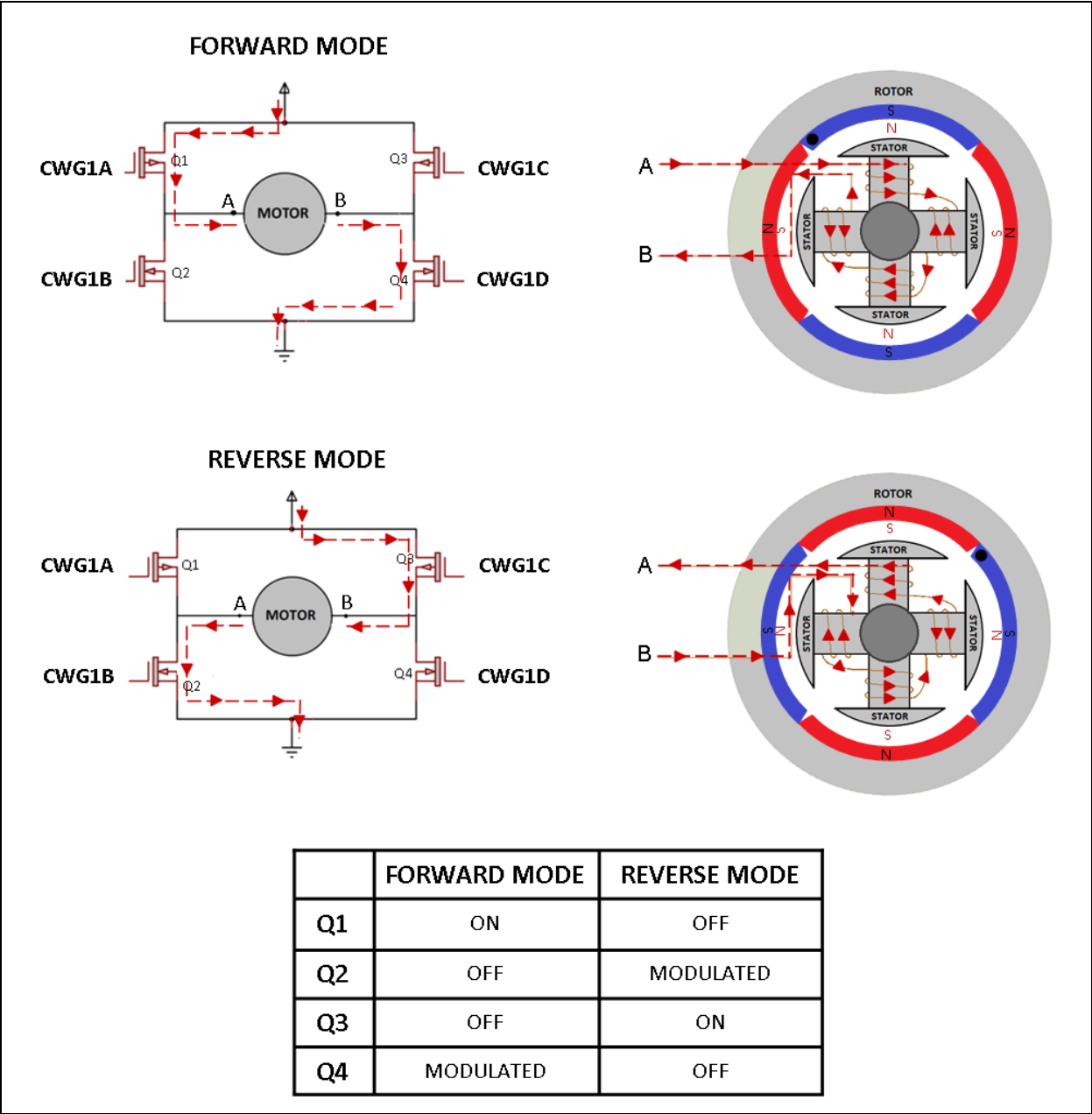


FIGURE 5: FORWARD AND REVERSE FULL-BRIDGE OPERATION



Full-Bridge Circuit

The schematic diagram of the full-bridge circuit seen in [Appendix E: “Circuit Schematic”](#) is primarily composed of two P-channel MOSFETs as high-side switches and two N-channel MOSFETs as low-side switches. The main advantage of using the P-channel MOSFET compared with the N-channel MOSFET as a high-side switch is the simplicity of gate-driving technique in the high-side switch position, thus reducing the cost of high-side gate-driving circuit. Transistor Q5 and resistors R1, R3 and R5 are configured as an emitter follower circuit, that acts as a level shifter to drive the P channel MOSFET Q1. Similarly, on the other arm of the full bridge, Transistor Q6 and resistors R2, R4, and R5 are configured as an emitter follower circuit that acts as a level shifter to drive the P-channel MOSFET Q3. When the CWG1A output is high, Q5 is conducting and the voltage across R1 relative to V_MOTOR provides negative voltage to charge the gate-to-source capacitance, and turns on Q1. Likewise, when CWG1C is high, Q6 is conducting and the voltage across R2 relative to V_MOTOR provides negative voltage to charge the gate-to-source capacitance and turns on Q3. The voltage across R1 and R2 when turning on Q1 and Q3 should be greater than the gate threshold voltage $V_{GS(TH)}$ and lower than the maximum gate-to-source voltage $V_{GS(max)}$ of Q1 and Q3. The voltage across gate to source of Q1 and Q3 can be calculated using [Equation 3](#) and [Equation 4](#). When CWG1A is low, Q5 is off and the gate-to-source capacitance voltage of Q1 discharges through R1 and turns off Q1. Likewise, when the CWG1C is low, Q6 is off and the gate to source capacitance of Q3 discharges through R2 and turns off Q3.

EQUATION 3: P-CHANNEL MOSFET (Q1) GATE-TO-SOURCE VOLTAGE (V_{GS})

$$V_{GS(Q1)} = - \frac{(V_{DD} - V_{BE(Q1)}) \times R1}{\frac{R3}{\beta_{DC}} + R5} \times \left(1 - \frac{1}{\beta_{DC}}\right)$$

$\beta_{DC} = Q5 \text{ DC Current Gain}$

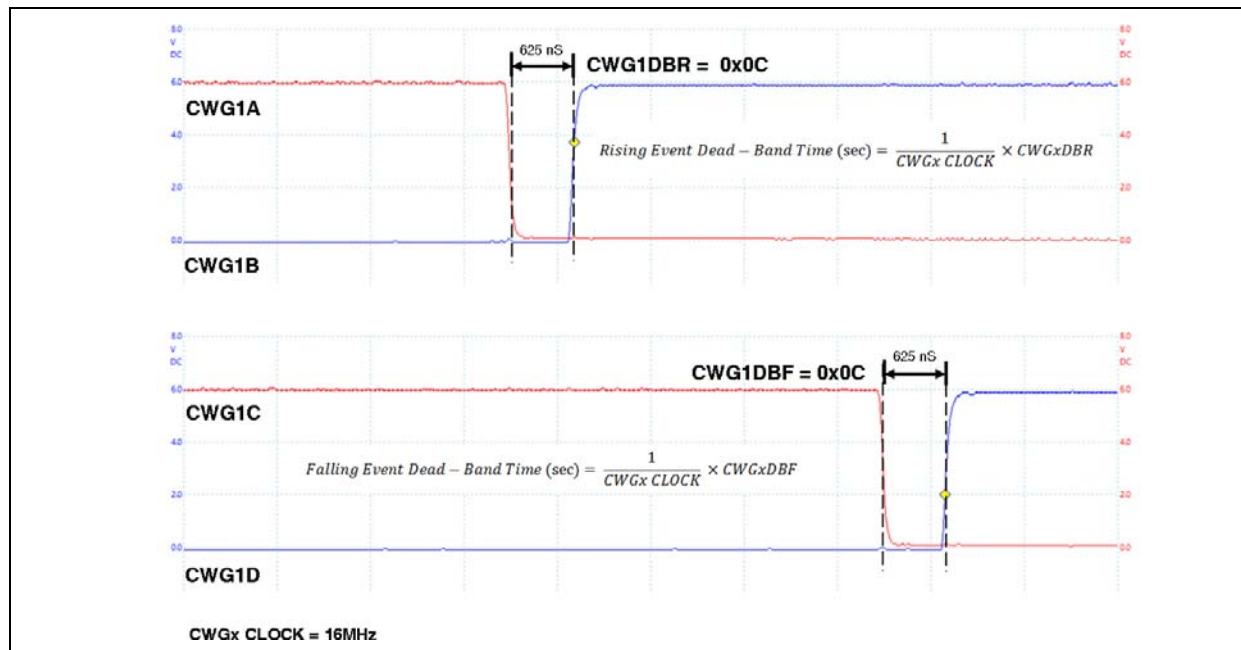
EQUATION 4: P-CHANNEL MOSFET (Q3) GATE-TO-SOURCE VOLTAGE (V_{GS})

$$V_{GS(Q3)} = - \frac{(V_{DD} - V_{BE(Q3)}) \times R2}{\frac{R4}{\beta_{DC}} + R5} \times \left(1 - \frac{1}{\beta_{DC}}\right)$$

$\beta_{DC} = Q6 \text{ DC Current Gain}$

The high and low-side switches (Q1 and Q2 or Q3 and Q4) can be switched-on at the same time (cross conduction). This kind of switching event should be avoided. Otherwise, it will create a current shoot-through that might damage the driver's components. To avoid this problem, a dead-band delay can be implemented. Using the CWG's counter registers, a dead-band delay can be imposed on the CWG outputs. This provides non-overlapping output signals that allow the high and low-side switches not to conduct at the same time. The CWG contains two 6-bit dead-band delay counters, one for the rising edge of the input source, and the other for the falling edge of the input source. This dead-band delay is timed by counting CWG clock periods from zero up to the value in the two CWG counter registers (CWG1DBR and CWG1DBF). [Figure 6](#) depicts the CWG outputs with dead-band delay.

FIGURE 6: CWG OUTPUT DEAD-BAND TIMER



Although dead bands are already provided, there is still a possibility that Q1 and Q2 or Q3 and Q4 conduct at the same time. This is because of the self turn-on phenomenon of the MOSFET related to the gate-to-drain internal miller capacitance. While Q1 is off and Q2 is modulating and at instant Q2 turns on, the drain voltage of Q1 and Q2 drops from V_MOTOR to 0V. The rapidly falling voltage rate of change (dv/dt) at the drain of Q1 produces current via parasitic gate-to-drain miller capacitance (C_{GD}) of Q1 to flow in R1 and internal gate-to-source capacitance (C_{GS}) of Q1. As a result, V_{GS} of Q1 can increase from 0 to a certain voltage level while it is in the turn-off state. If V_{GS} reaches the threshold voltage V_{TH} of Q1, Q1 will falsely turn on and cross conduction of Q1 and Q2 will happen. On the other hand, while Q1 is off and Q2 is off and at instant Q1 turns on, the drain voltage of Q1 and Q2 rise from 0 to V_MOTOR. The rapidly rising voltage rate of change (dv/dt) at the drain of Q2 produces current, via C_{GD} of Q2, to flow in R6 and C_{GS} of Q2. As a result, V_{GS} of Q2 can increase from 0 to a certain voltage level while it is in the turn off state. If the V_{GS} reaches V_{TH} of Q2, Q2 will falsely turn on and cross conduction of Q1 and Q2 will happen. The other arm of the full-bridge circuit is also susceptible in the occurrence of this phenomenon.

The coupling effect at the V_{GS} can be roughly calculated using Equation 5, where R is total gate resistance of the MOSFET in the circuit, C_{rss} is equal to C_{GD}, C_{iss} is equal to C_{GS} + C_{GD}, and dv/dt is the low-side switch drain-to-source voltage rate of change.

EQUATION 5: V_{GS} COUPLING EFFECT CALCULATION

$$V_{GS(MILLER)} = \frac{dv}{dt} \times R \times C_{rss} \left\{ 1 - e^{\left(\frac{-V_{MOTOR}}{\frac{dv}{dt} \times R \times C_{iss}} \right)} \right\}$$

In order to reduce the internal coupling effect, the external capacitor is connected across the gate-to-source of the MOSFETs. In the schematic diagram, C1, C2, C3 and C4 are connected across the gate-to-source of Q1, Q2, Q3 and Q4, respectively. These capacitors increase the effective C_{iss} for each respective MOSFET. For example, when C1 is connected across the gate-to-source of Q1, the effective value of C_{iss} of Q1 is equal to C_{GS} + C_{GD} + C1. Looking back at Equation 5, when C_{iss} increases, the coupling effect at the gate of Q1 decreases.

In this application, the key parameters in selecting MOSFETs are based on the device $RDS_{(on)}$ (On-Resistance) and Q_G (Total Gate Charges). Ideally, the N-channel and the P-channel MOSFETs in the full-bridge circuit should have the same $RDS_{(on)}$ and Q_G in order to attain the optimal switching performance. Therefore, it is convenient to choose a complementary pair of a P-channel and a N-channel device in order to match these parameters. However, this is impossible due to the difference of construction of the two MOSFETs. The chip size of the P-channel must be two to three times that of the N-channel in order to match the N-channel $RDS_{(on)}$ performance, but the larger the chip size, the larger the effect on its dynamic performance, such as Q_G . On the other side, when the P-channel has the same Q_G as the N-channel, P-channel and N-channel have the same chip size, but the P-channel has larger $RDS_{(on)}$ than the N-channel. Because of this trade off, it is imperative to choose which parameter between $RDS_{(on)}$ and Q_G will mostly affect the switching performance of the MOSFET. The decision is determined based on the MOSFET's operating switching frequency. At high-frequency (greater than 50 kHz) operation, switching losses are dominant. When Q_G of the P-channel is comparable with the N-channel MOSFET, it will significantly reduce the total MOSFET power losses. Otherwise, at low-frequency (less than 50 kHz) operation, conduction losses are dominant. When $RDS_{(on)}$ of the P-channel is comparable with the N-channel MOSFET, it will significantly reduce the total MOSFET power losses. In this motor driver solution, the switching frequency is 15.625 kHz, therefore, the P-channel and the N-channel MOSFETs were chosen through their comparable $RDS_{(on)}$. See [Table 2](#).

**TABLE 2: MOSFET CHARACTERISTICS
(Q_G AND RDS_{on})**

MOSFET TYPE	P/N	Q_G	RDS_{on}
P-Channel	FDS6375	26 nC	0.024 Ω at $V_{GS} = -4.5V$
N-Channel	NDS8425	11 nC	0.022 Ω at $V_{GS} = 4.5V$

Overcurrent Detection

Exceeding the motor's maximum allowable torque loading can cause the motor to stall and the winding to take the full current. To protect the motor from overheating, Fault detection for overcurrent and stalling must be implemented.

To implement overcurrent detection, RSHUNT is added to the drive circuitry that gives a voltage corresponding to the current flowing in the motor winding. The voltage drop across this resistor varies linearly with respect to the motor current. The voltage is fed to the inverting input of the comparator and compared with a certain reference voltage. This reference voltage is based on the product of RSHUNT resistance and the maximum allowable stall current of the motor. The reference voltage can be provided by the FVR which can be also narrowed down further by the DAC. In this manner, very small reference voltage can be used, allowing the RSHUNT resistance to be kept low. Keeping the resistance low reduces the RSHUNT power dissipation. If the RSHUNT voltage exceeds the reference, the comparator output will trigger the Auto-shutdown feature of the CWG and the CWG Output will be inactive as long as a fault exists.

Overtemperature Detection

Overtemperature can be detected using the device on-chip temperature indicator. The indicator measures the device temperature, which will correspond to the temperature in its environment with some delay.

The indicator is used to measure the device temperature between $-40^{\circ}C$ and $+85^{\circ}C$. The internal circuit of the temperature indicator produces a variable voltage relative to temperature using internal transistor junction threshold voltage. This voltage is converted to digital form by the ADC. The ADC result will be used to determine the actual temperature reading defined by [Equation 6](#). For a more accurate temperature indicator reading, a single-point calibration is implemented. Refer to Application Note AN1333, "Use and Calibration of the Internal Temperature Indicator" (DS01333) for more details regarding the calibration process.

EQUATION 6: TEMPERATURE READING CALCULATION

$$\text{Temperature Reading} = \frac{0.659 - \left[\frac{V_{DD}}{\text{mode}} \left\{ 1 - \frac{ADC_{RESULT}}{(2^n - 1)} \right\} \right]}{0.00132} - 40$$

Where:

High-Range mode = 4

Low-Range mode = 2

N = number of bits of ADC Resolution

ADC_{RESULT} = ADRES Register Value

After obtaining the calibrated ADC Result, it will be compared with the desired maximum temperature limit. When the ADC result exceeds the maximum temperature limit, the output of the CWG disables. The implementation of overtemperature detection in the code uses a Timer 1 interrupt to check the temperature every time the timer expires.

Table 3 summarizes the ADC Result that the temperature indicator produces relative to the temperature.

TABLE 3: TEMPERATURE INDICATOR ADC RESULT SUMMARY

Temperature (°C)	VTEMP	8-bit ADC Result	10-bit ADC Result
-40	2.364	121	484
-30	2.4168	123	494
-20	2.4696	126	505
-10	2.5224	129	516
0	2.5752	131	527
10	2.628	134	538
20	2.6808	137	548
30	2.7336	139	559
40	2.7864	142	570
50	2.8392	145	581
60	2.892	147	592
70	2.9448	150	603
80	2.9976	153	613
85	3.024	154	619

Note 1: VDD = 5V, Mode = High Range.

OUTER LOOP

The outer loop shown in [Figure 2](#) provides control of the motor's speed. The objective in controlling the motor's speed is to maintain the speed of the motor at the desired value under various conditions such as change in load demand, disturbances and temperature drift.

[Figure 7](#) shows the firmware's new PWM duty cycle calculation process in order to retain the motor's constant speed. The speed reference is based on the previously discussed references (see Speed Reference section) and the actual speed measured by the SMT. The SMT is a 24-bit counter/timer with advanced clock and gating logic, which can be configured for measuring a variety of digital signal parameters such as pulse width, frequency, duty cycle, and the time difference between edges on two input signals. Measuring the motor's output frequency can be done through the use of SMT Period and Duty Cycle Single Acquisition mode. In this mode, either the duty cycle or period of the SMT Signal can be acquired relative to the SMT clock. The SMT counts the number of SMT clocks present in a single period of motor rotation and stores the result in SMT Captured Period Register (SMTCPR). Using the SMTCPR, the actual frequency of the motor can be obtained as shown in [Equation 8](#). Combining [Equation 7](#) and [Equation 8](#) to relate SMTCPR output count to RPM yields [Equation 9](#).

EQUATION 7: RPM CALCULATION

$$RPM = \frac{120 \times \text{Frequency}}{\text{Number of Poles}}$$

EQUATION 8: SMT CAPTURED PERIOD REGISTER CALCULATION

$$SMTCPR = \frac{SMT \text{ Clock Source}}{\text{Motor Frequency}}$$

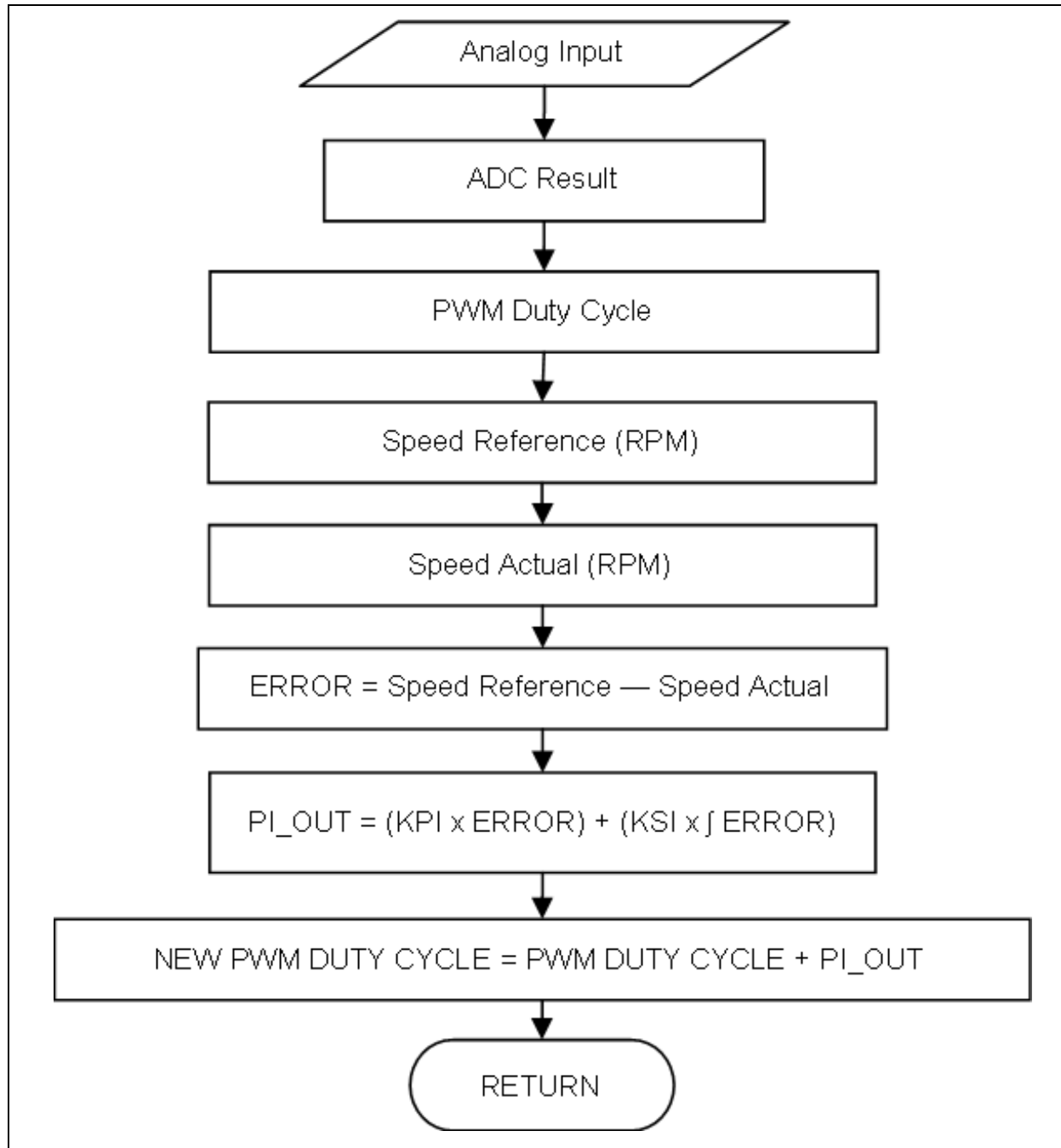
EQUATION 9: COMBINED EQUATION TO CALCULATE ACTUAL SPEED

$$\text{Actual Speed (RPM)} = \frac{120 \times SMT \text{ Clock Source}}{\text{Number of Poles} \times SMTCPR}$$

When the speed reference is compared with the actual speed, it will yield an error. This error can be positive or negative, which indicates that the actual speed is higher or lower than the set reference. The error is feed to a Proportional-Integral (PI) controller. The PI controller is a firmware algorithm that calculates a value that compensates the variation in speed. Refer to

Application Note AN937, "Implementing a PID Controller Using a PIC18 MCU" (DS009237) for more information about the theory and tuning of PI and PID controllers. When the compensating value is calculated, it will add or subtract to the initial PWM duty cycle to produce a new PWM duty cycle value.

FIGURE 7: SPEED CONTROL CALCULATION



PERFORMANCE

Figure 8 shows the motor speed step response and Figure 9 shows the motor overall speed performance using a driver solution based on the PIC16F1613 microcontroller.

FIGURE 8: MOTOR SPEED STEP-RESPONSE

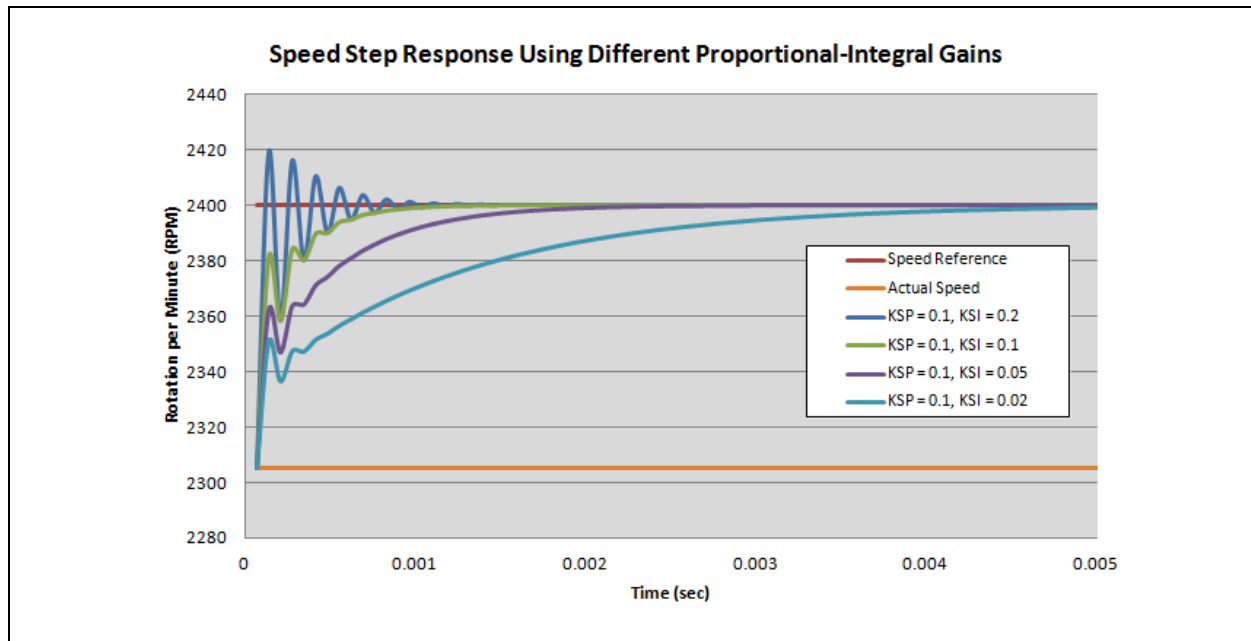
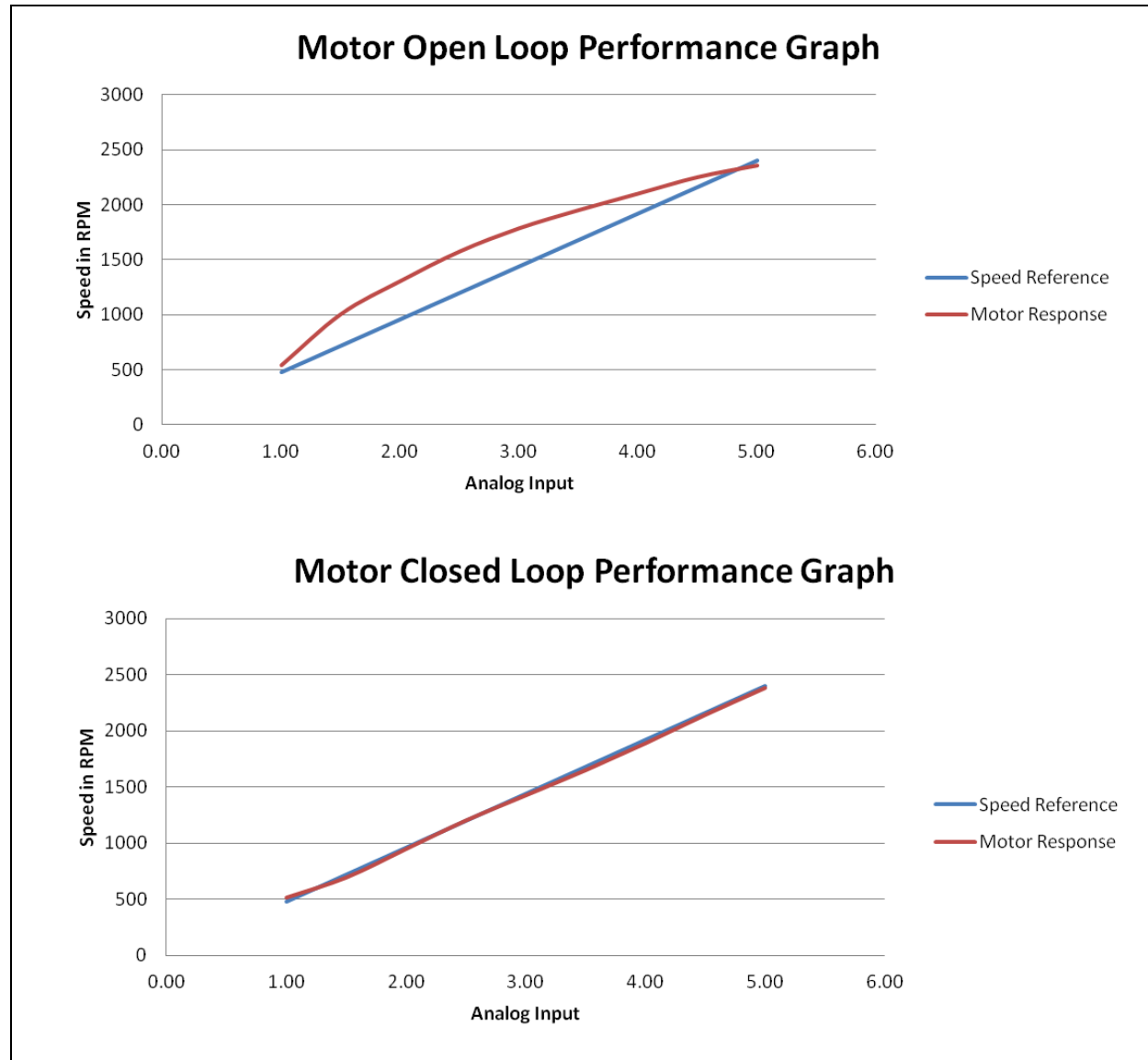


FIGURE 9: OPEN LOOP VS. CLOSED LOOP MOTOR PERFORMANCE GRAPH

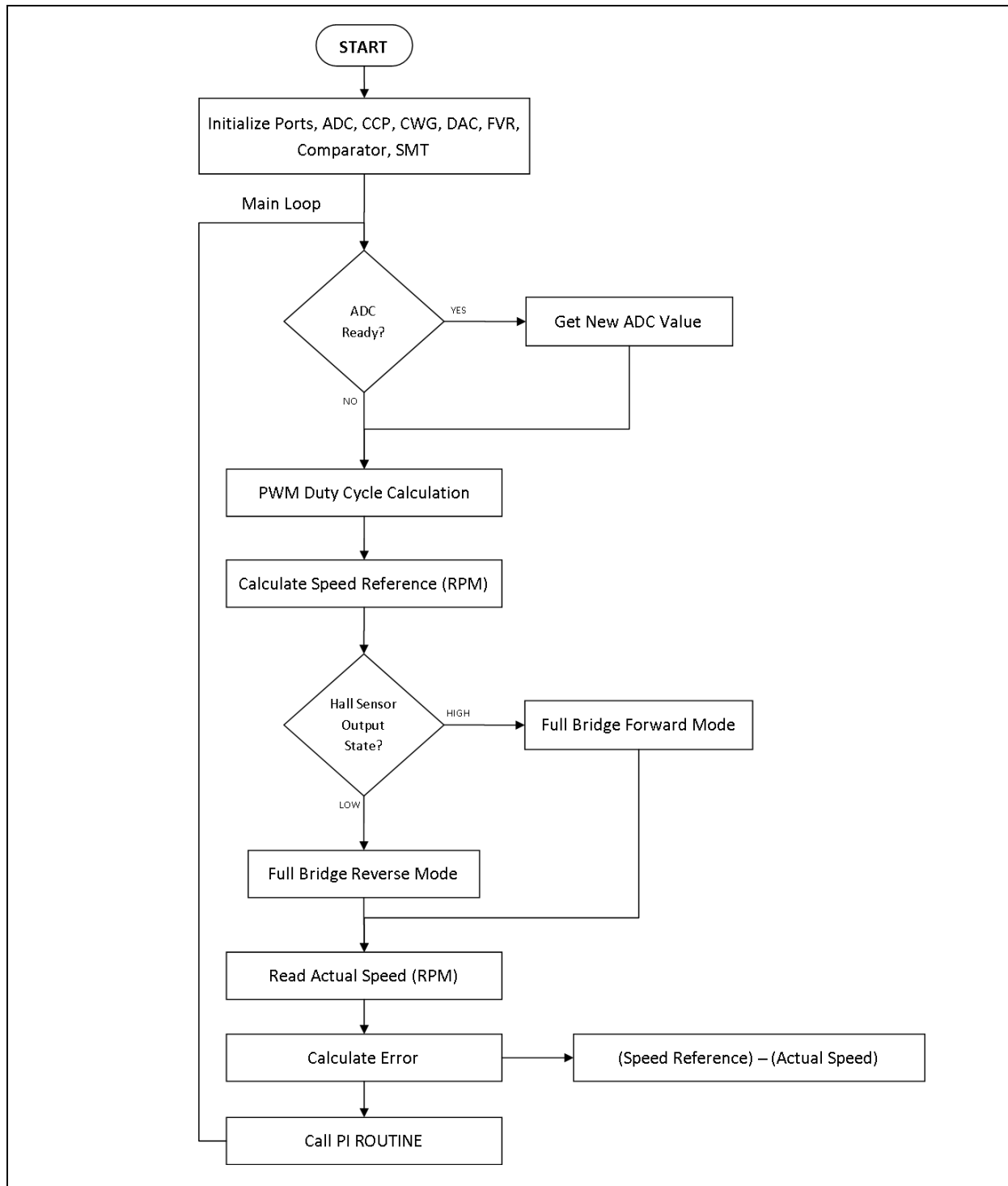


CONCLUSION

In cost-sensitive motor control applications an efficient and flexible microcontroller can have significant impact. Device efficiency can be measured against the level of integrated peripherals to optimize the control task along with the number of pins/memory and the size of package. In addition, ease of use and time to market are important, especially if variants of the designs are required. This application note describes how a low-cost microcontroller meets these requirements. By using the PIC16F1613, the motor driver can set desired speed reference, predict the rotor position, implement control algorithm, measure actual motor's speed and impose fault detection.

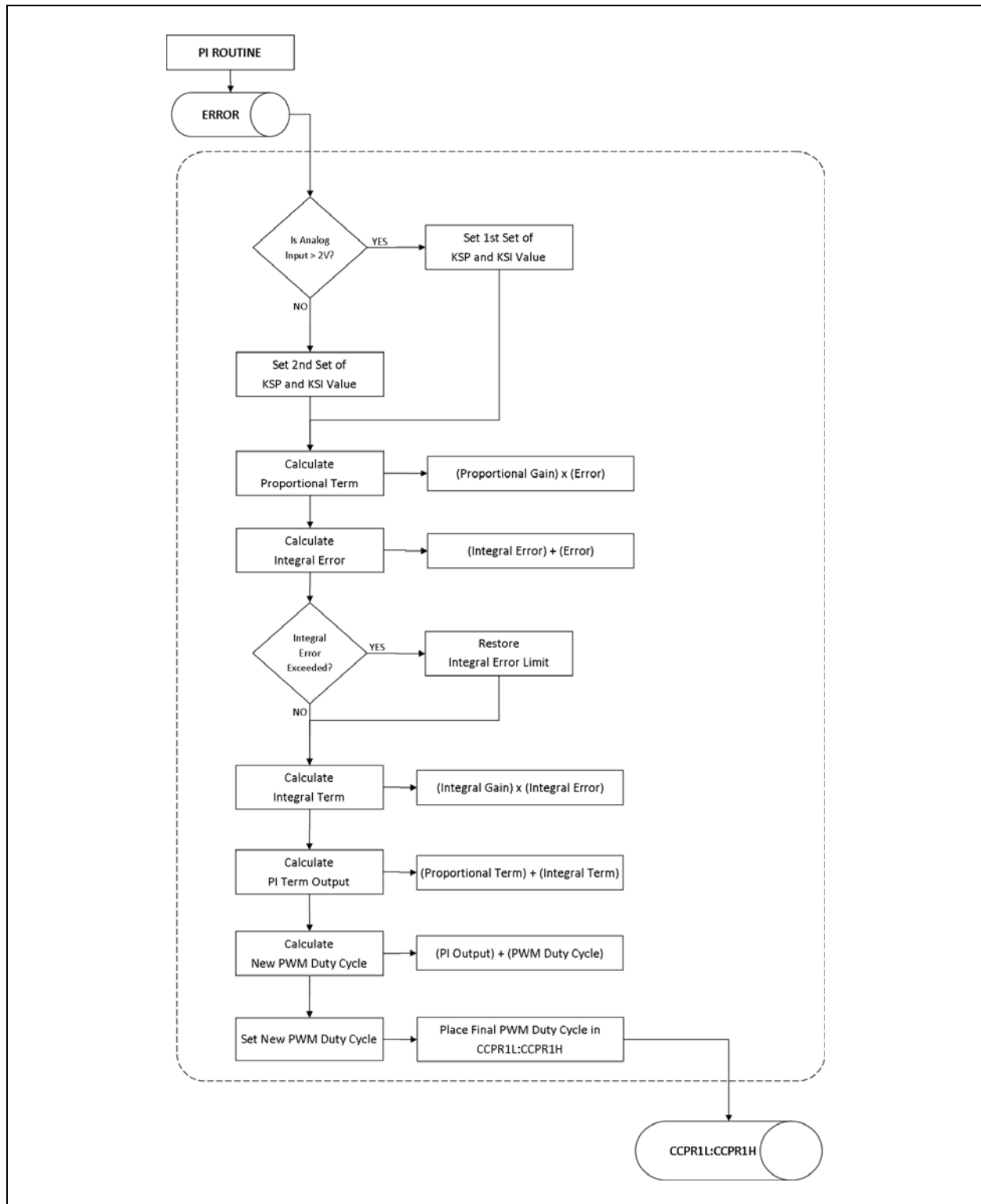
APPENDIX A: MOTOR CONTROL FLOWCHART

FIGURE A-1: MAIN LOOP ROUTINE



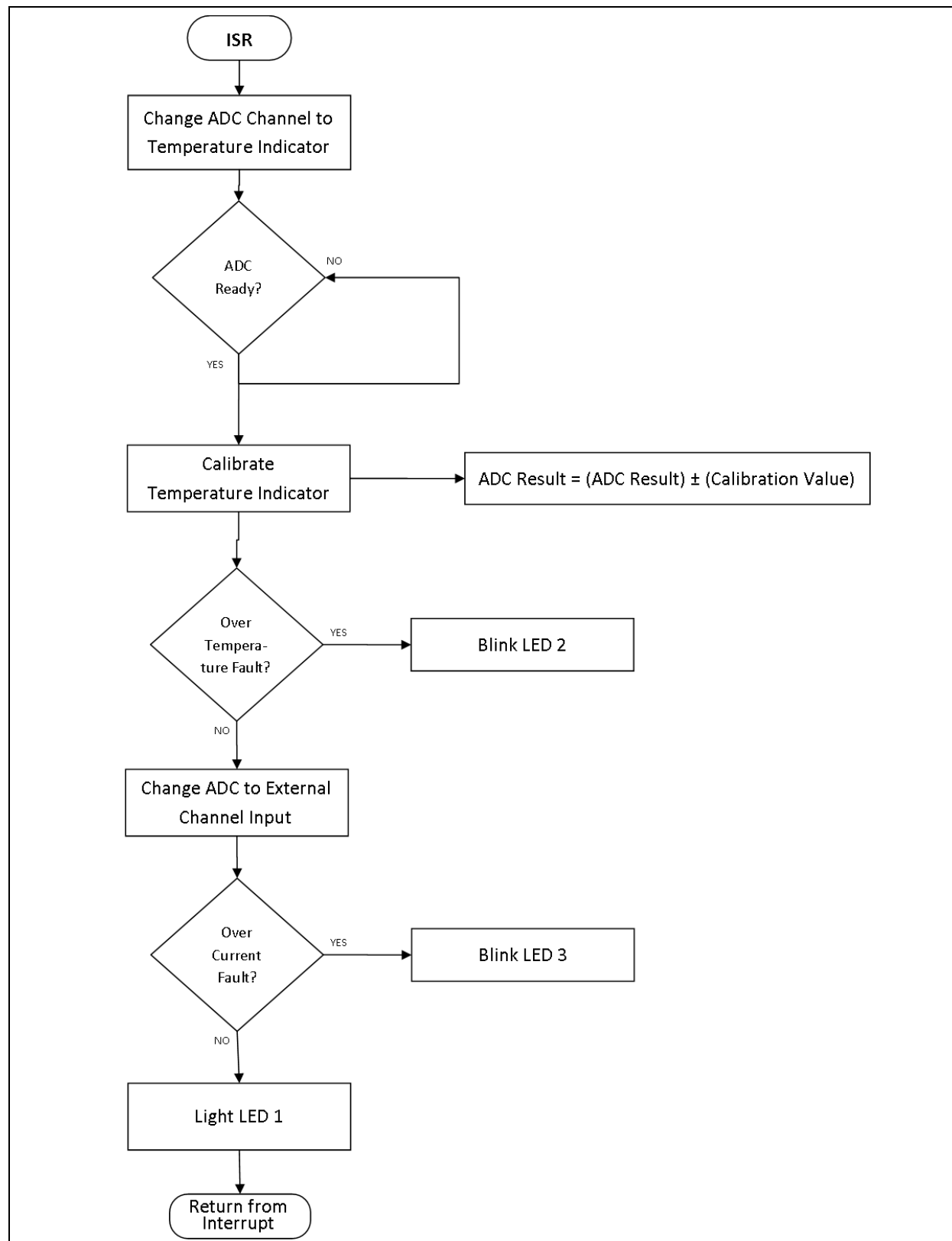
APPENDIX B: SPEED CONTROLLER FLOWCHART

FIGURE B-1: PI CONTROLLER ROUTINE



APPENDIX C: INTERRUPT FLOWCHART

FIGURE C-1: INTERRUPT SERVICE ROUTINE



APPENDIX D: SOURCE CODE LISTING

The latest software version can be downloaded from the microchip web site (www.microchip.com). The user will find the source code appended to the electronic version of this application note. The latest version is V2.0.

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